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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,552	02/26/2004	Hiroyoshi Kuge	8008-1050	3414

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EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	**PAPER NUMBER**
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,552	KUGE ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-10* is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *1,2 and 5-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 sheets*. 5/5/5 8/26/4 2/26/4
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the design automation apparatus including a memory unit, computing section, circuit simulator, detecting section and layout section recited in claims 5-6, and the circuit simulator recited in claims 7-10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because the "repeater" depicted in figure 9 should be given a reference number that corresponds to the description of figure 9 in the specification [page 26], this would clarify the subject matter depicted and conclusively distinguish the subject matter from the prior art figure referred to [page 25, line 5]. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be

canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1:121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Language to illuminate that a semiconductor IC device, apparatus, method and program employ a test, involving boundary scan or JTAG, is encouraged.

The abstract of the disclosure is objected to because the grammar is confusing. For example, "for transfer a" [line 5] and "or so" [line 13] is not clear. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: "Input" [page 2, line 14] should be changed to --Output--.

Appropriate correction is required.

Claim Objections

Claims 1-2 and 5-10 are objected to because of the following informalities: as per claim 1, "a" [line 3, first occurrence] should be deleted to clarify subsequent antecedent basis; there is no antecedent basis for "said plurality" [line 8]; and, it is not clear that a cell is indeed empty if it has a repeater circuit [lines 9-12], thus what is meant by a semiconductor IC device having an empty cell having a repeater circuit therein is confusing since the claim does not appear to be definitively written in product by process form. As per claim 2, what is meant by 'previously prepared" [line 6] is not clear in terms of the semiconductor IC device structure; and, what is meant by "said empty cell" [line 9] is confusing since the previous feature recites that an optimal

repeater circuit is "laid out in said one empty cell or said plurality of empty cells" [lines 8-9]. As per claims 5, 7, and 9, "cells" [line 7, 7, 6, respectively] should be singular. As per claims 6, 8, and 10, "optical" [line 10, 11, 11, respectively] should be changed to --optimal--. As per claims 7 and 9, there is no antecedent basis for "said circuit simulator" [lines 18-19, 17, respectively]. Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 9-10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In order for the algorithm of the "program" to recite statutory subject matter, one of the requirements is that the claims must be encoded on a computer readable medium. Therefore, the language should be amended to include statutory subject matter, for example, "A program embodied in a computer readable medium for..." or "A program comprising a computer readable medium for...", or similar wording.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Okawa [Patent Abstracts of Japan Publication Number 2000022081].

Okawa discloses a semiconductor IC device comprising: predetermined I/O cells provided in an I/O area in a peripheral portion of a chip and to be connected to external pins; signal wirings which transfer a test signal to said I/O cells and are provided in said I/O area in a layout direction of said I/O cells; and at least one empty cell where said signal wirings run and which is to be a transfer path for said test signal, is provided in said I/O area, and has a repeater circuit that receives said test signal and outputs said

test signal; wherein said I/O cells include a boundary-scan register circuit and said signal wirings include a wiring for a signal to be supplied to said boundary-scan register circuit; wherein said I/O cells include a scan flip-flop circuit for a scan path test signal to be supplied to said scan flip-flop circuit [Abstract; figure 3; paragraphs 0016 and 0017].

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Jones ["JTAG Clock & Control Signal Distribution Scheme"]

Jones discloses a semiconductor IC device comprising: predetermined I/O cells provided in an I/O area in a peripheral portion of a chip and to be connected to external pins; signal wirings which transfer a test signal to said I/O cells and are provided in said I/O area in a layout direction of said I/O cells; and at least one empty cell where said signal wirings run and which is to be a transfer path for said test signal, is provided in said I/O area, and has a repeater circuit that receives said test signal and outputs said test signal; wherein said I/O cells include a boundary-scan register circuit and said signal wirings include a wiring for a signal to be supplied to said boundary-scan register circuit; wherein said I/O cells include a scan flip-flop circuit for a scan path test signal to be supplied to said scan flip-flop circuit [the whole document].

Allowable Subject Matter

Claims 5-10 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance: the prior art of record does not disclose, teach, or suggest, taking claim 7 as exemplary, a design automation method for a semiconductor IC using a computer having a memory unit which stores I/O cell layout position information, I/O cell size information, I/O cell test terminal information, technology information including design information, and information on a repeater circuit to be laid out in an empty cell for each type of I/O cell on a chip which are to be connected to external pins, said method comprising the particular steps recited in their totality.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Narayanan et al. [U.S. Patent #5,983,376] disclose scan insertion including buffers being inserted in empty space [column 7, lines 31-33]. Sonohara [U.S. Patent Application Publication #2004/0006754 and Japan Application #2002-199192] discloses arranging buffers in empty areas [figures 4-5 and 9-10]. Dirks et al. [U.S. Patent #7,000,163 B1] disclose optimized buffering for JTAG boundary scan nets [figures 3 and 5]. Amekawa [U.S. Patent #6,983,436 B2 Japan Application #2002-336473] disclose using empty space for correcting crosstalk [element 5]. Osaki et al. [U.S. Patent #6,564,362 B2] disclose arranging boundary scan registers, I/O cells and buffer cells [Abstract].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEIGH M. GARBOWSKI
PRIMARY EXAMINER